

United States Patent [19]

Foss et al.

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[54] DYNAMIC RANDOM ACCESS MEMORY
USING IMPERFECT ISOLATING
TRANSISTORS

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[57] ABSTRACT

Apparatus and methods for controlling the sensing of bit lines which facilitates the distribution of bit line charging current to be distributed any time, and facilitates the fast raising of the sense nodes to full logic levels. An embodiment is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors, having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, apparatus connected to the bit line and the sense nodes for imperfectly isolating the sense nodes from the bit line whereby current can leak therethrough, apparatus for enabling the sense amplifier and for disabling the isolating apparatus and thereby removing the isolation between the sense amplifier and the bit line, whereby current passing through the sense amplifier to the sense nodes is enabled to charge the bit line capacitance through the isolating apparatus to predetermined logic voltage level.

Related U.S. Application Data

[63] Continuation of Ser. No. 680,747, Apr. 5, 1991, abandoned.

[30] Foreign Application Priority Data

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[52] U.S. CL 365/203; 365/149.

[58] Field of Search 307/530; 365/149, 208,
365/203, 222, 189.01, 204, 207, 205

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17 Claims, 3 Drawing Sheets

